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(71) Applicant: Rockwell International Corporation
2230 East Imperial Highway
El Segundo, California 90245(US)

(72) Inventor: Smithson, Richard Allen
4059 Jeffrey
Yorba Linda California 92686(US)

(74) Representative: Wagner, Karl H.
P.O. Box 246 Gewuerzmuehlstrasse 5
D-8000 München 22(DE)

(54) **Synchronization system for digital data.**

(57) A digital signal synchronization system including a digital signal source for supplying an input digital signal, and a plurality of substantially identical integrating circuits, each connected to the digital signal source for integrating the signal for a predetermined time. A plurality of clock sources are also provided, each connected to a corresponding one of the integrating circuits, so that each integrating circuit begins integrating the digital signal at a different time. Decision means are connected to the output of each of the integrating circuits for electing one of the integrating circuits according to a predetermined criteria.

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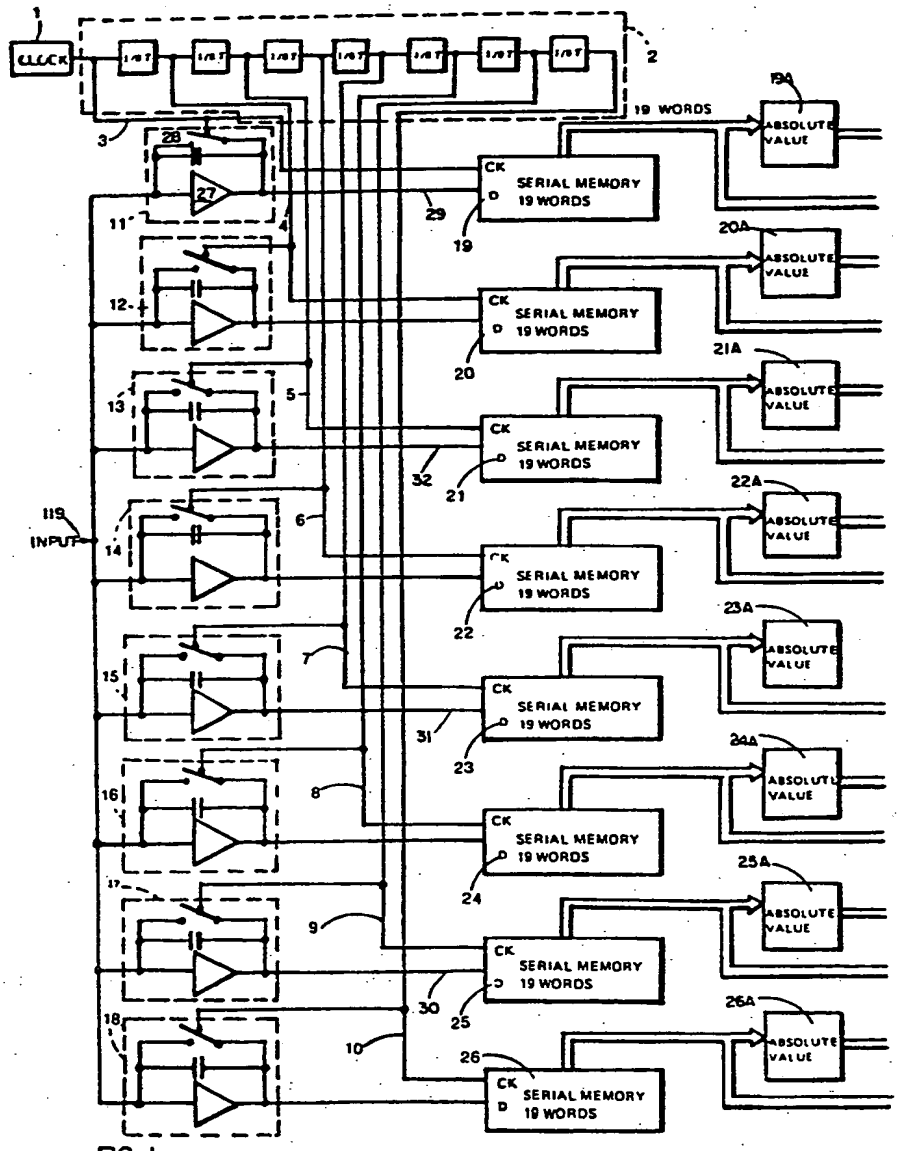

CLOCK
1/8T
2
19 WORDS
3
28
27
11
4
12
5
13
119
INPUT
14
6
15
7
16
8
17
9
18
10
CK
D
SERIAL MEMORY
19 WORDS
19
20
21
22
23
24
25
26
29
30
31
32
19A
20A
21A
22A
23A
24A
25A
26A
ABSOLUTE
VALUE

FIG. 1a

PF79E96

SYNCHRONIZATION SYSTEM FOR DIGITAL DATA

The invention herein described was made in the course of or under a contract or subcontract thereunder, with the United States Navy.

Field of the Invention

The invention relates to systems for the detection and synchronization of data presented in digital waveforms, and in particular for synchronizing a digital signal with the clock timing of an incoming digital signal with noise.

Background of the Invention

There are numerous methods for the detection and synchronization of data for use in noisy environments, and in particular techniques using integration for the detection of data in distinct state signal waveforms. One such method is presented in U.S. Patent No. 3,864,583 which provides a pair of integration circuits forming an integrator for each state of the digital signal with the integrators being alternately actuated. In such prior art for a two-state signal, two integrators are provided with a clocking system to alternately actuate pairs of the integrators. A subsequent amplitude comparison is then used to determine the date represented by the digital signal.

Phase-lock loop techniques are used to establish data synchronization by comparing input noisy digital data with a reference clock in a phase detector. The reference clock phase is adjusted to establish a minimum phase error with respect to the incoming data. Phase-lock techniques have the disadvantage of requiring many clock cycles to establish synchronization resulting in data being lost during the synchronization process.

U.S. Patent No. 4,012,598 describes a receiver with a synchronizer which operates by selecting synchronized samples of a digital signal making use of a tap delay line. The most recent samples of the post signals are then stored and synchronized samples are detected by decoding sequence transitions.

U.S. Patent No. 4,088,833 describes another multiphase sampling device used as a carrier detector in a multipoint communication system. A tapped delay line is used together with an amplitude difference decision circuit for providing an indication that the data signal has been received.

U.S. Patent No. 3,602,826 describes an apparatus for detecting signal level variations in the presence of noise or other background phenomena. The signals are sequentially sampled according to a predetermined scanning sequence and processed in parallel channels on a synchronized element by element basis to derive an amplitude representation of the level variations occurring over maximum and minimum time intervals. These amplitude representations are then compared as an indication of whether they represent actual information signal or simply noise.

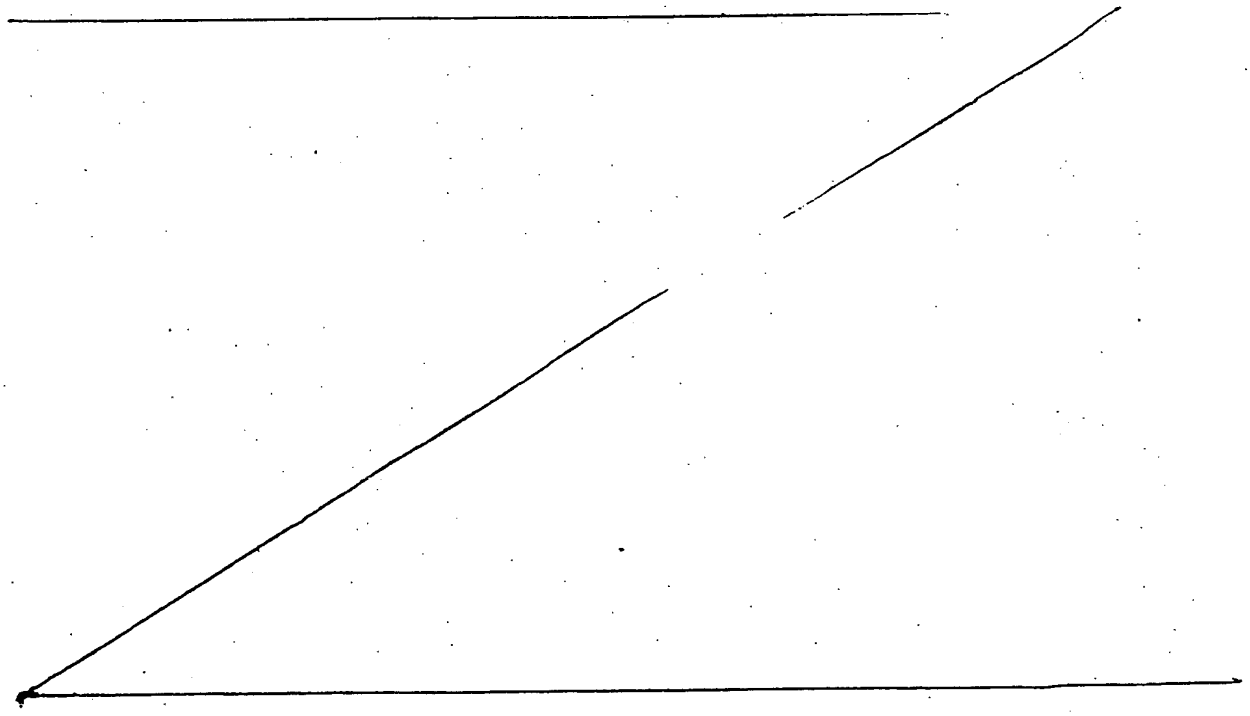
Other pertinent patents include U.S. Patent Nos. 3,502,905; 3,602,826; 3,716,780; and 4,007,330.

Each of these prior art techniques generally have disadvantages: U.S. Patent No. 4,012,598 does not provide integration thereby making the system sensitive to noise. U.S. Patent 3,864,583 provides integration but does not address the problem of establishing clock data synchronization. U.S. Patents No. 4,088,833 and 3,602,826 pertains to determining if a singal is present and does not address the problem of determining the information content contained in the signal.

Summary of the Invention

Briefly, and in general terms, the invention provides a digital signal synchronization system comprising a digital signal source for supplying an input digital signal, a plurality of substantially idential integrating circuits, each connected to the digital signal source for integrating the signal for a predetermined time. The invention further provides a plurality of clock sources, each connected to a corresponding one of the integrating circuits so that each integrating circuit begins integrating the digital signal at a different time, and decision means connected to the output of each of the integrating circuits for selecting one of the integrating circuits according to a predetermined criteria.

The novel features which are considered as characteristic for the invention are set forth in particular in the appended claims. The invention itself, however, both as to its construction and its method of operation, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.



Brief Description of the Drawing

FIG. 1 a and b is a highly simplified block diagram of a first embodiment of the digital signal synchronization system according to the present invention:

FIG. 2 is a timing diagram of a clock signal associated with the synchronizing system shown in FIG. 1;

FIG. 3 is a highly simplified diagram of the waveforms associated with the integrators shown in FIG 1;

FIG. 4 is a graph showing the output of the summing circuits shown in FIG. 1b;

FIG. 5 a and b is a detailed block diagram of a second embodiment of the present invention;

FIG. 6 is a timing diagram of the clock signal associated with the synchronizing system shown in FIG. 5;

FIG. 7 is a block diagram of the third embodiment of the present invention; and

FIG. 8-11 are flow-charts of the program used for the microprocessor in the embodiment of FIG. 7.

Description of Preferred Embodiment

Turning now to FIG. 1, consisting of sheets 1a and 1b, there is shown a block diagram of a first embodiment of the synchronization system according to the present invention. There is shown a clock 1 operated at near the incoming data clock rate at the input 119. The delay line 2 is connected to the clock 1 and provides eight distinct clock phases that equally divide the clock period as shown in FIG. 2.

FIG. 2 shows the timing diagram of the clock and all of its resulting phases (FIGs. 2a-2b) from the output of the delay line 2. Each of these clock signals is connected to and synchronizes a corresponding matched filter 11-18, shown in FIG. 1.

A matched filter such as the filter 11 consists of an integrator 27 and a discharge switch 28. Each integrator integrates the incoming noisy data from the input 119 for the duration of one clock period. At the end of each clock phase (FIG. 2a-2h), the integrator is discharged and the value of the integrator just prior to being discharged is transferred to the D input of a corresponding serial memory 19-26, respectively. The data in the respective serial memory is shifted one word when the integrator transfer occurs.

FIG. 3 is a highly simplified diagram of the waveforms associated with the integrators shown in FIG. 1. FIG. 3 shows waveforms 29 through 32 which are typical waveforms for the output of integrators 11, 17, 15, and 13 respectively.

The top series of waveforms shows a predetermined digital code word represented by waveform 59, and the noisy data 118 superimposed over the waveform 59. The noisy data 118 is applied to the data input 119. Each of the subsequent blocks of waveforms shows a clock phase, the waveform applied to the integrator, the data which is stored in the serial memory, and the absolute value derived from the data stored in the serial memory.

The first block of waveforms shows the data corresponding to the output of integrator 11, which is a channel 180° out of phase with the data clock. The next block of waveforms corresponds to the output of integrator 17 and illustrates a channel 90° out of phase with the data. The next block corresponds to the output of integrator 15 and corresponds to a channel in phase with the data. The last block of waveforms shown in FIG. 3 is associated with the output of integrator 13 and illustrates a channel minus 90° out of phase with the data. The signals actually transferred to the serial memories 19, 25, 23, and 21 are shown as waveforms 33-36 respectively.

The output of serial memories 19-26 are connected to absolute value circuits 19A-26A respectively. The absolute values of the words stored in the serial memories 19, 25, 23, and 21 are computed by absolute value circuits 19A, 25A, 23A, and 21A respectively. The sum of the absolute values of each of the words in each of the memories is computed by circuits 35-42 for each serial memory.

FIG. 4 shows the value of the sum of absolute values for each channel. Sum 47 is the largest and coincides with the channel with the best synchronized clock phase (phase 5).

The largest decode circuit 51 determines the largest sum of absolute values. The largest decode circuit directs switch 52 to connect the channel with the largest absolute value to the decoder circuits 53.

The decoder circuit shown in 53 will detect the presence of a digital code word such as waveform 59 shown in FIG. 3 in the noisy data such as represented by waveform 118. The circuit 53 consists of a convolution circuit 55, a summer circuit 56, and a threshold circuit 57. The convolution circuit 55 is connected to the switch 52 and processes each word in the selected serial memory with respect to the expected digital code word. If the expected digital code bit is a logical "1" the serial memory word is multiplied by +1 and added to the summer 56. If the code bit is a "0", then the serial memory word is multiplied by -1 and added to the summer device 56. The summer 56 accumulates the sum of each word in the selected serial memory in this manner. The sum 60 is then compared to a detection threshold in circuit 57. If the sum is greater than the threshold, then the code word is said to have been found in the noisy data 118.

An alternative detection circuit 54 can also be used to detect digital data of waveform 118 one bit at a time. This detector compares the data with the last word in the serial memory using a comparator circuit 58. If that word is greater than the threshold, the data is said to be a logical "one" and if it is less than the threshold, it is said to be logical "zero".

Turning now to FIG 5a and b, there is shown a hardware block diagram of a second embodiment of the present invention.

The multiphase clock generator 60 is another embodiment of the circuit described by reference numeral 2 in FIG. 1. The 8x clock circuit 70 generates a clock 61 at eight times the frequency of the incoming data rate. Counter 71 overflows once every eight clock cycles. The counter overflow is shifted into shift register 72. Shift register 72 is clocked with the eight times clock frequency 61 thus producing the multiphase clock shown in FIG 6. The first clock phase signal is applied to line 62.

The noisy data input 119 is applied to and digitized by the analog to digital converter (ADC) 73. The output of the ADC, the data on line 74, represents a sampled version of the data on input line 119. The sampled data on line 74 is then presented to each of the eight processing channels 75 through 82 simultaneously. Each of the channels 75-82 is

essentially the same and is typified by the circuit forming channel 1 and shown in detail in Figure 5a in block 75.

Data on line 74 is added to the contents of register 84 with adder 83 on each cycle of the eight times clock, thus integrating the digitized waveform. When channel reset time occurs, indicated by a low pulse on line 62, the feedback from register 84 to adder 83 is disabled by gate 85, so that the register 84 is loaded with data on line 74 resulting in an integrator reset. When the integrator is reset, the contents of register 84 is clocked into shift register 86. The clock on line 62 causes the contents of shift register 86 to be shifted one word.

Adders 87 and 88 and register 89 compute and save the sum of the absolute values of the data in shift register 86. Adder 87 adds the absolute value of the new data from register 84 to the data in register 89 while adder 88 substracts the absolute value of the last word of data in shift register 86, thus register 89 contains the sum of the absolute values of the data in shift register 86. Adder 87 adds the data from register 84 to the data on line 90 if the data from register 84 has a positive sign, or subtracts the data from register 84 from the data on line 90 if the data from register 84 has a negative sign. Thus the absolute value of the data from register 84 is always added to line 90. Adder 88 subtracts the data on line 91 from the data on the lines 92 if the data on the lines 91 is positive. Alternatively, adder 88 adds the data on lines 91 if the data on lines 91 is negative. Thus adder 88 always subtracts the absolute value of the data on line 91.

The output of processing channel 75 is connected to circuit 92. The circuit 92 functions to find the best synchronized channel by finding the channel with the largest absolute value. The address of the best synchronized channel is stored in register 95. Register 96 contains the absolute value of the data associated with the channel stored in register 95.

The operation of circuit 92 begins at clock time one when register 96 is loaded with the absolute value of the data on channel 1 and register 97 is loaded with the address channel "one". On the next cycle of the 8x, clock multiplexer 93 connects channel 2 to the magnitude comparator 94. If

channel-2 has a larger absolute value than is stored in register 96, the comparator 94 causes the absolute value of channel-2 to be stored in register 96 and address "two" to be stored in register 97. In a similar manner channels 3 through 8 are compared. After clock eight, register 96 contains the absolute value of the best synchronized channel. The contents of register 97 are transferred to register 95 before register 97 is reset for the next cycle, thus register 95 contains the address of the best channel through the next cycle.

The register 95 directs multiplexer 96 as to which channel to connect to the output data line "output". If the sign bit of the last word in the shift register of the best synchronized channel is a one indicating a negative number in 2's complement notation, then the detected data is said to be a logical "zero" and if the sign bit is a zero indicating a positive number in 2's complement notation, then the detected data is said to be a logical "one".

Comparator 99 compares the best channel address contained in register 95 with the current clock address line 100. When a comparison occurs in comparator 99, a recovered clock pulse is generated on line 101.

Magnitude comparator 102 compares the magnitude of the absolute value of the best channel contained in register 96 with a predetermined magnitude indicative of data being received. If the magnitude of the absolute value is greater than the predetermined magnitude on line 103, register 104 is set indicating valid data is contained in the channel indicated by register 95.

FIG. 7 is a third embodiment of the present invention using a microprocessor 109. The flow chart describing the operation is shown in FIGS 8-11. The implementation shown can either detect a code word in the input noisy data or decode a digital data stream.

The analog-to-digital converter (ADC) 108 is operated at a sample rate of eight times the expected incoming data rate. The sample rate clock is achieved by dividing the clock 106 with the divide by N circuit 107. The ADC is connected to the microprocessor bus 113. This connection allows the microprocessor to read the digitized noisy data.

The read only memory (ROM) 111 connected to the microprocessor bus contains the program shown in FIGS. 8-11. The random access memory 112 also connected to the bus, is used by the microprocessor for variable data storage. The input-output device (I/O), 110 is used to indicate the bit stream or the presence of the code word in the noisy data.

The program for operating the microprocessor 109 is shown in the flow chart FIGS. 8-11, and is self-explanatory.

In summary, the present invention allows the use of a matched filter detection scheme for short sequence of noisy data which could be associated with teletype, telemetry-transmissions where it is important to receive all data bits transmitted.

Prior to the present invention phase-lock techniques were used for clock synchronization when integrated and dump matched filters were used to detect noisy digital data. Phase-lock techniques have an inherent disadvantage of requiring several clock cycles to establish synchronization. The present invention circumvents this disadvantage and allows for the detection of all data bits.

The present invention may be used to detect many forms of digital signals, where the signal takes on two distinct states and may contain additive noise. The integration incorporated in the present invention decreases the influence of additive noise resulting in an increase in detection sensitivity. The storage of the

multi-integrate and dump matched filter prevents the loss of data during the synchronization interval normally associated with phase-lock techniques.

While the invention has been illustrated and described as embodied in a synchronization system for digital data, it is not intended to be limited to the details shown, since various modifications and structural changes may be made without departing in any way from the spirit of the present invention.

Without further analysis, the foregoing will so fully reveal the gist of the present invention that others can, by applying current knowledge, readily adapt it for various applications without omitting features that, from the standpoint of prior art, fairly constitutes essential characteristics of the generic or specific aspects of this invention, and, therefore, such adaptations should and are intended to applying current knowledge, readily adapt it for various applications without omitting features that, from the standpoint of prior art, fairly constitutes essential characteristics of the generic or specific aspects of this invention, and, therefore, such adaptations should and are intended to be comprehended within the meaning and range of equivalence of the following claims.

What is claimed is:

79E96

Claims

1. A digital signal synchronization system comprising:

a digital signal source for supplying an input digital signal;

a plurality of substantially identical integrating circuits each connected to said digital signal source for integrating the signal for a predetermined time;

a plurality of clock sources each connected to a corresponding one of said integrating circuits so that each integrating circuit begins integrating said digital signal at a different time; and

decision means connected to the output of each of said integrating circuits for selecting one of said integrating circuits such that said clock signal associated with said one of said integrating circuits is the synchronized clock signal associated with said input digital signal.

2. A system as defined in Claim 1, wherein said decision means functions to select said one of said integrating circuits having the output with the greatest absolute value.

3. A system as defined in Claim 1, when said integrating circuits comprises integrate and dump matched filters.

4. A system as defined in Claim 1, wherein each of said clock sources has a frequency identical with the data rate of the input digital signal.

5. A system as defined in Claim 1, wherein each of said clock sources has a different phase.

6. A system as defined in Claim 1, further comprising convolving means connected to the output of said selected one of said integrating circuits.

7. A system as defined in Claim 1, further comprising threshold detection means connected to the output of said selected one of said integrating circuits.

8. A system as defined in Claim 1, wherein said integrating circuit comprises a serial memory for storing a plurality of words in information representing the successive integrations of said input signal.

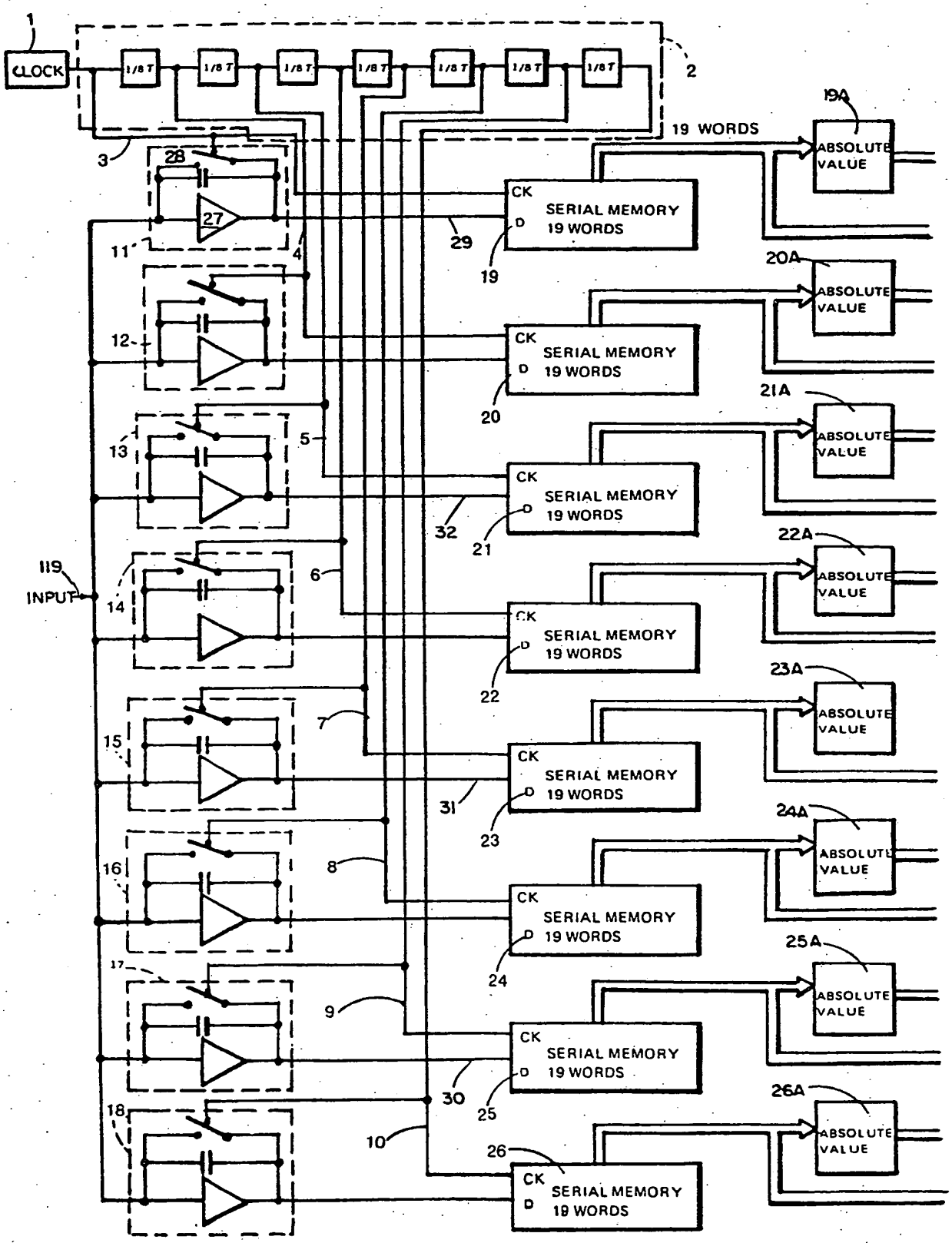

CLOCK
1/8 T
19 WORDS
SERIAL MEMORY 19 WORDS
CK
D
ABSOLUTE VALUE
INPUT
19A
20A
21A
22A
23A
24A
25A
26A

FIG. 1a

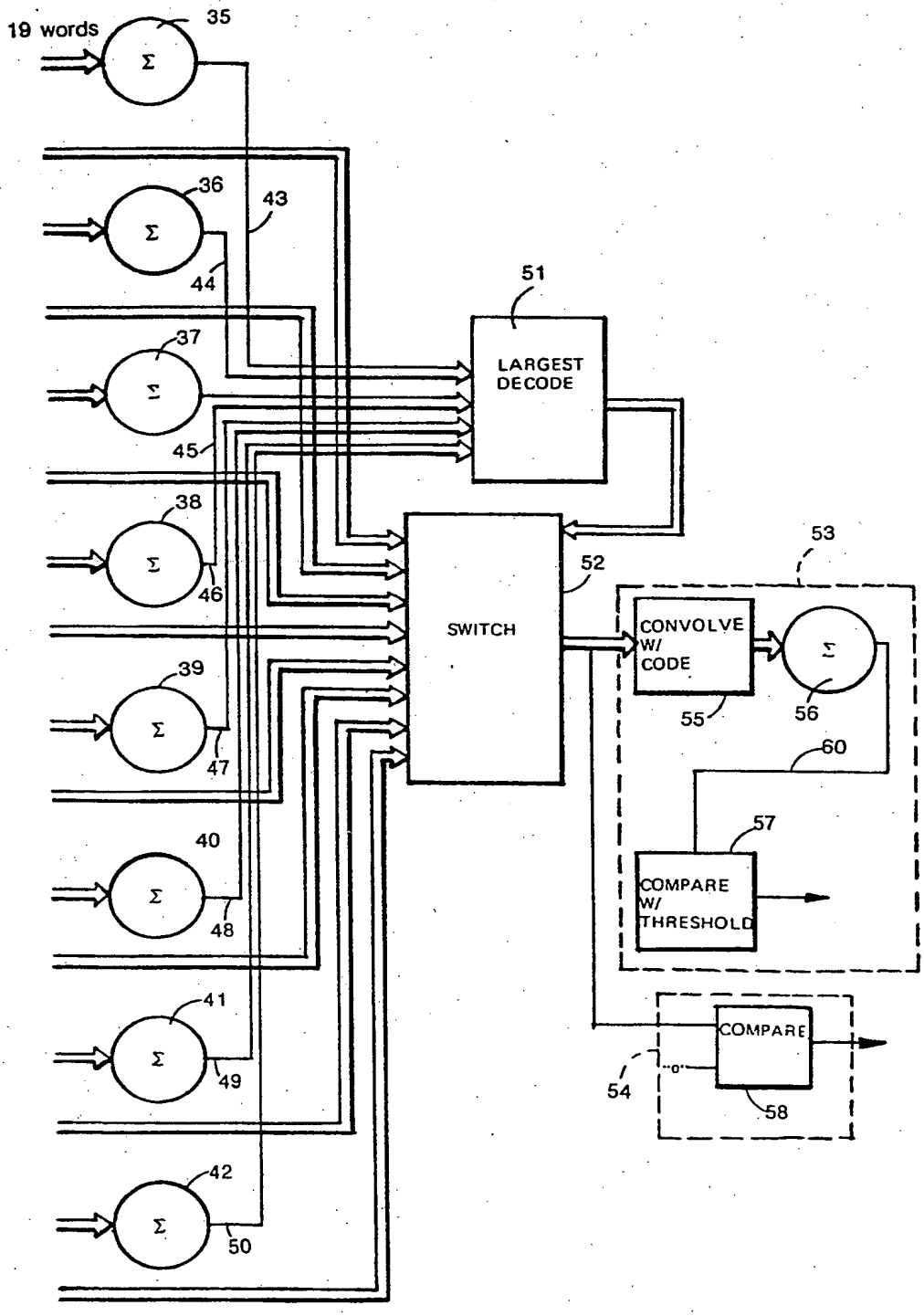

19 words
35
Σ
36
43
44
51
LARGEST DECODE
37
45
38
46
SWITCH
52
53
CONVOLVE W/ CODE
55
56
39
47
60
57
40
COMPARE W/ THRESHOLD
48
41
49
COMPARE
54
58
42
50

FIG. 1b

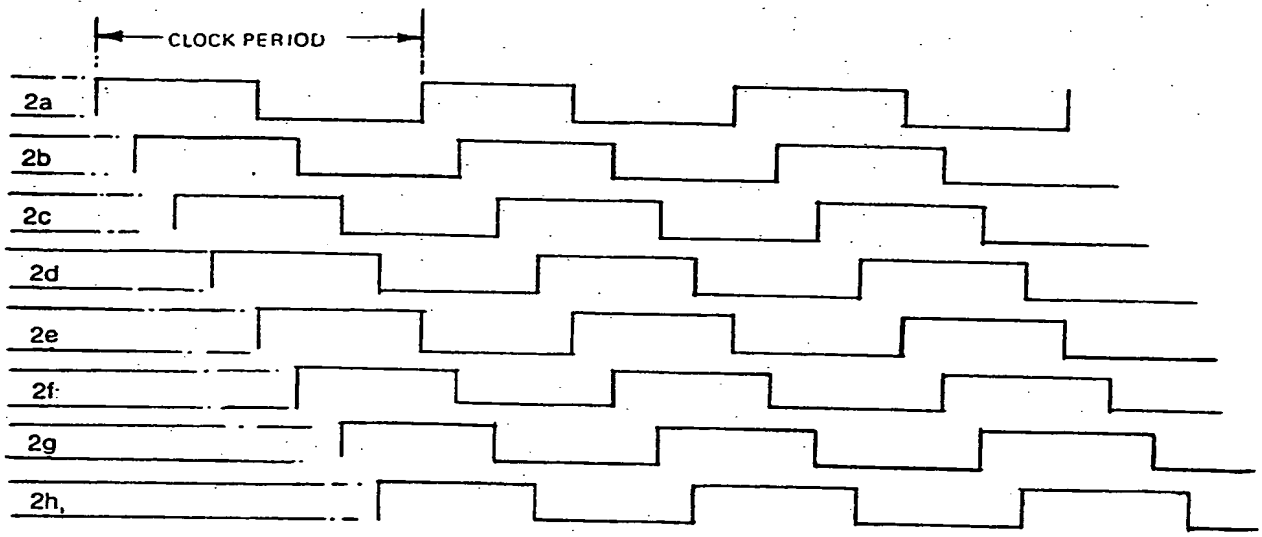

CLOCK PERIOD
2a
2b
2c
2d
2e
2f
2g
2h,
CLOCK TIMING

FIG. 2

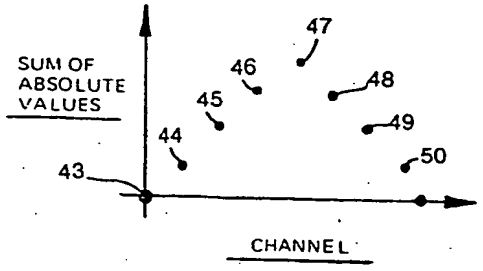

SUM OF ABSOLUTE VALUES
43
44
45
46
47
48
49
50
CHANNEL

FIG. 4

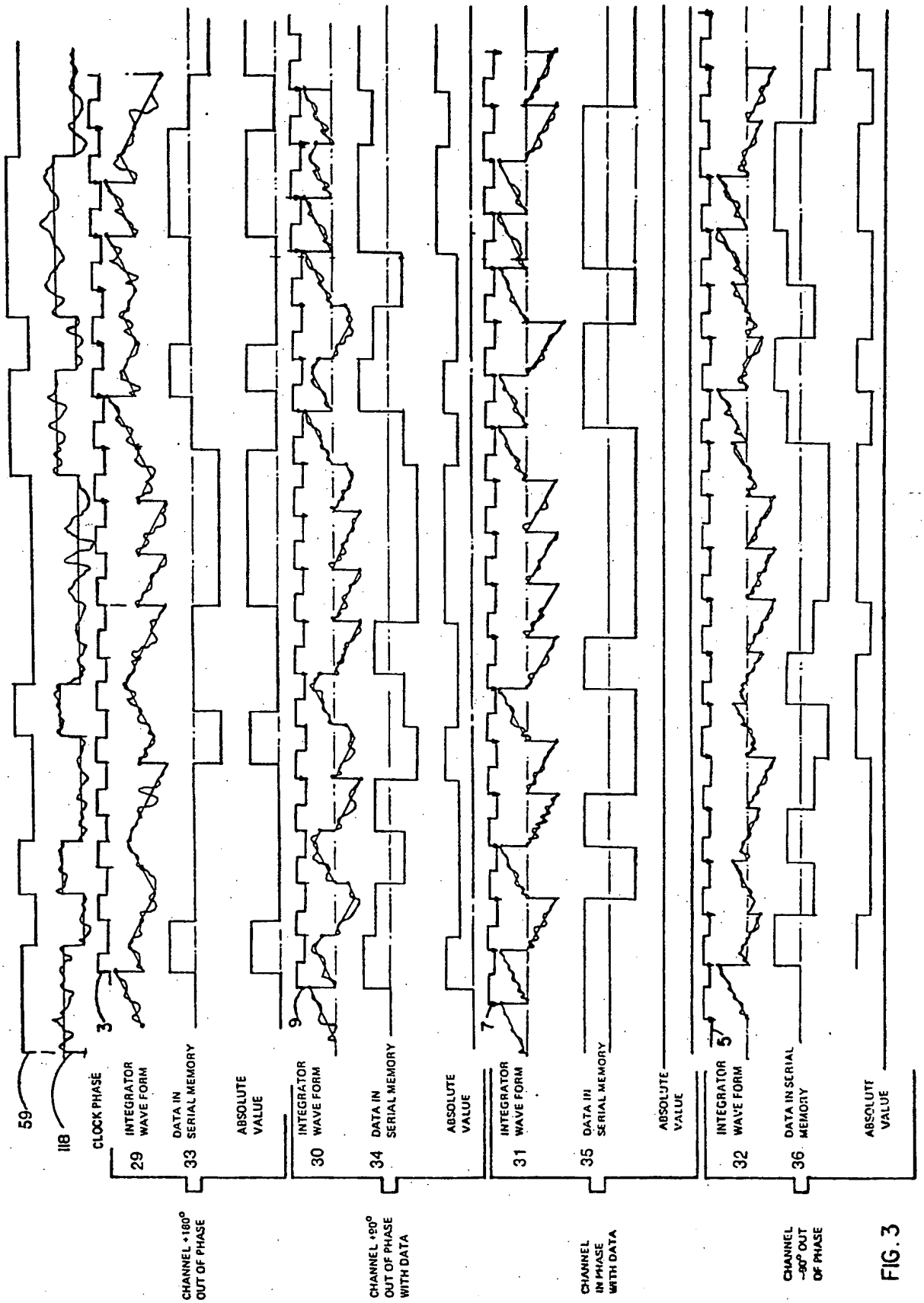

59
118
CLOCK PHASE
29 INTEGRATOR WAVE FORM
3
33 DATA IN SERIAL MEMORY
ABSOLUTE VALUE
CHANNEL +180° OUT OF PHASE
30 INTEGRATOR WAVE FORM
9
34 DATA IN SERIAL MEMORY
ABSOLUTE VALUE
CHANNEL +90° OUT OF PHASE WITH DATA
31 INTEGRATOR WAVE FORM
7
35 DATA IN SERIAL MEMORY
ABSOLUTE VALUE
CHANNEL IN PHASE WITH DATA
32 INTEGRATOR WAVE FORM
5
36 DATA IN SERIAL MEMORY
ABSOLUTE VALUE
CHANNEL -90° OUT OF PHASE

FIG. 3

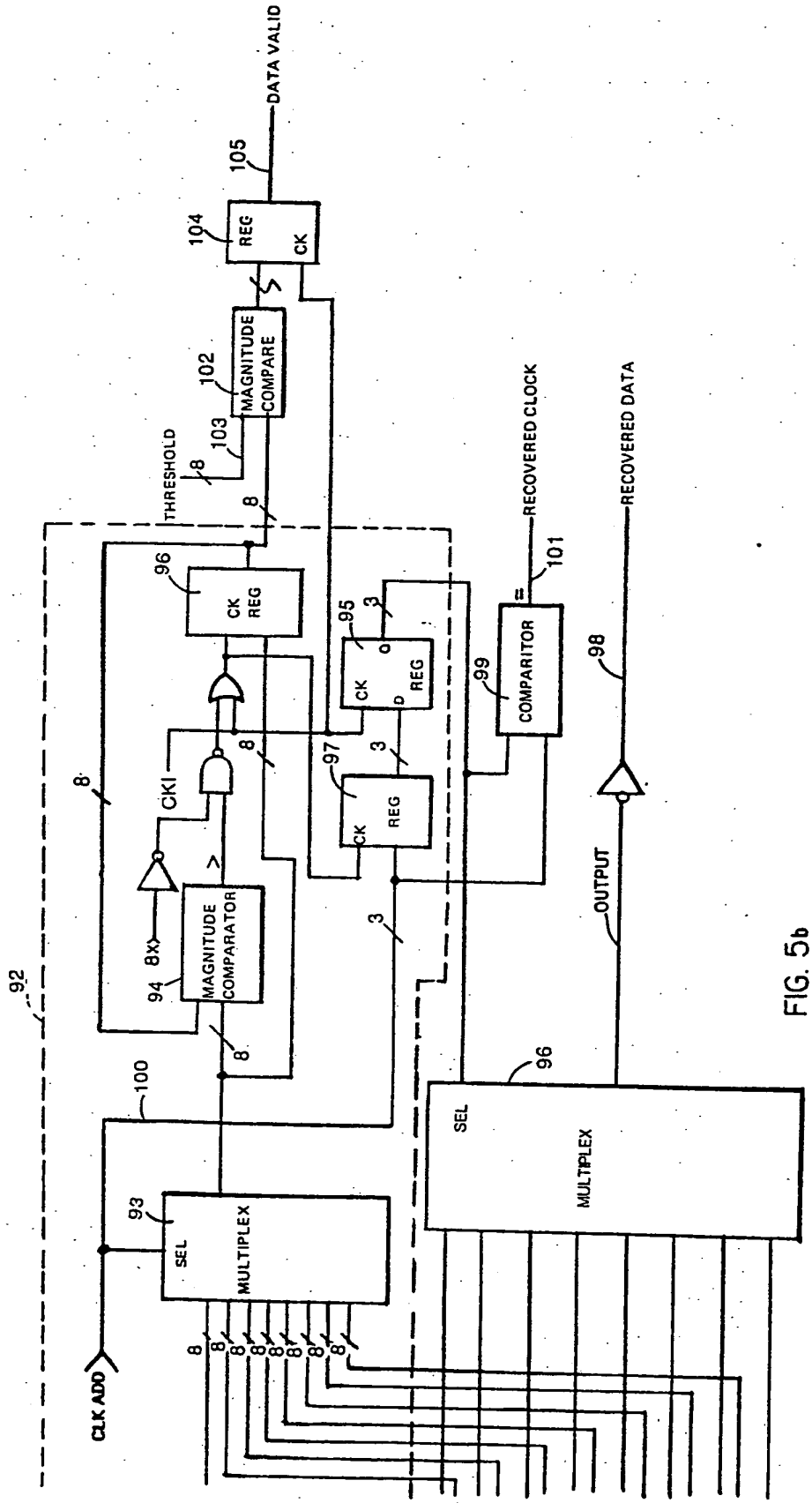

DATA VALID
105
104
REG
CK
MAGNITUDE COMPARE
102
103
THRESHOLD
8
RECOVERED CLOCK
RECOVERED DATA
101
96
CK REG
95
3
CK
REG
D
Q
98
99
COMPARITOR
97
CK1
>
8X
MAGNITUDE COMPARATOR
94
92
OUTPUT
100
SEL
MULTIPLEX
93
CLK ADD

FIG. 5b

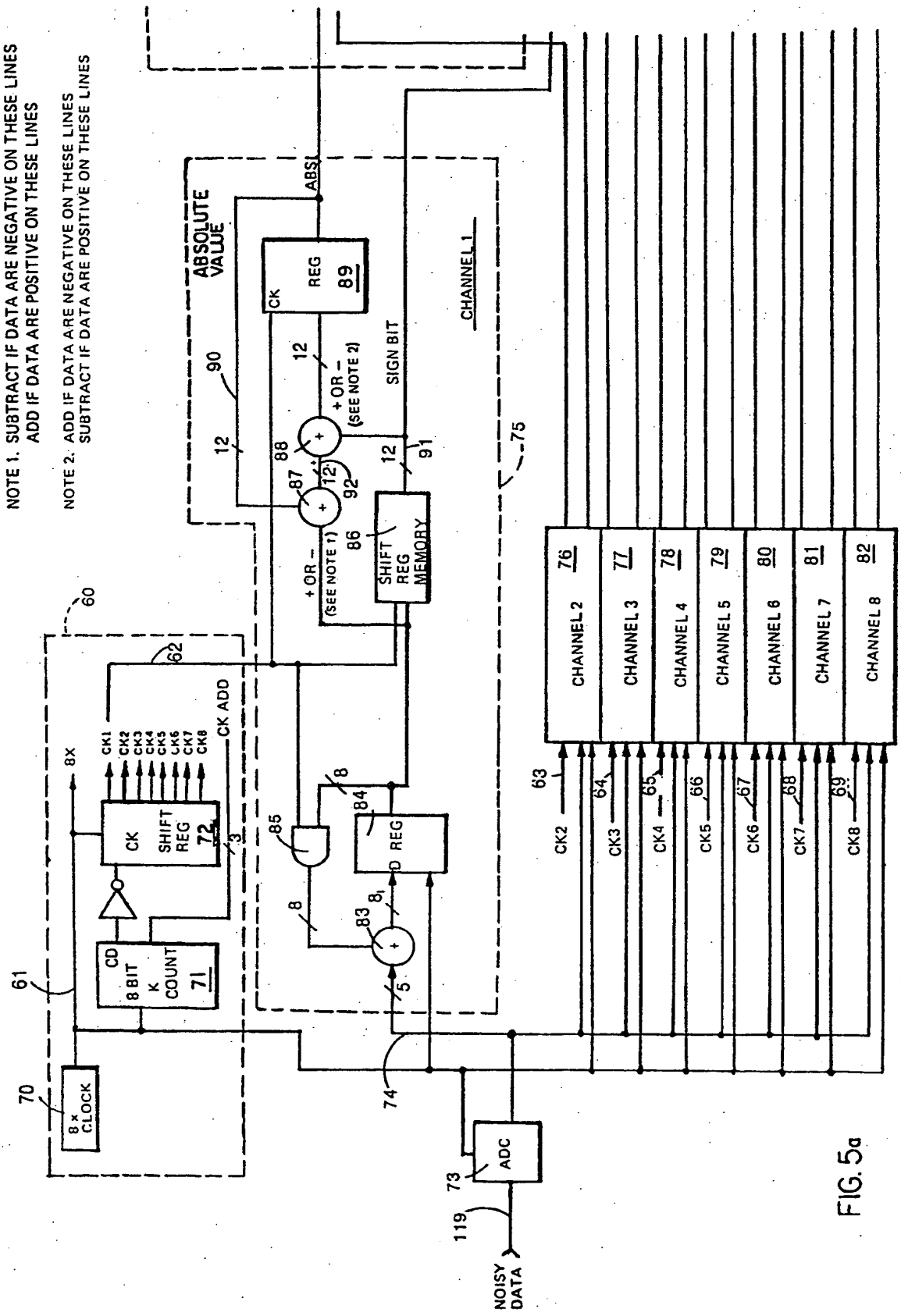

NOTE 1. SUBTRACT IF DATA ARE NEGATIVE ON THESE LINES
ADD IF DATA ARE POSITIVE ON THESE LINES
NOTE 2. ADD IF DATA ARE NEGATIVE ON THESE LINES
SUBTRACT IF DATA ARE POSITIVE ON THESE LINES
ABSOLUTE VALUE
ABS
CK
REG 89
SIGN BIT
CHANNEL 1
+ OR − (SEE NOTE 2)
+ OR − (SEE NOTE 1)
SHIFT REG MEMORY 86
D REG 84
CHANNEL 2 76
CHANNEL 3 77
CHANNEL 4 78
CHANNEL 5 79
CHANNEL 6 80
CHANNEL 7 81
CHANNEL 8 82
8X
CK1 CK2 CK3 CK4 CK5 CK6 CK7 CK8
CK ADD
SHIFT REG 72
CD 8 BIT K COUNT 71
8 x CLOCK
ADC
NOISY DATA
60
61
62
63
64
65
66
67
68
69
70
73
74
75
83
85
87
88
90
91
92
119

FIG. 5a

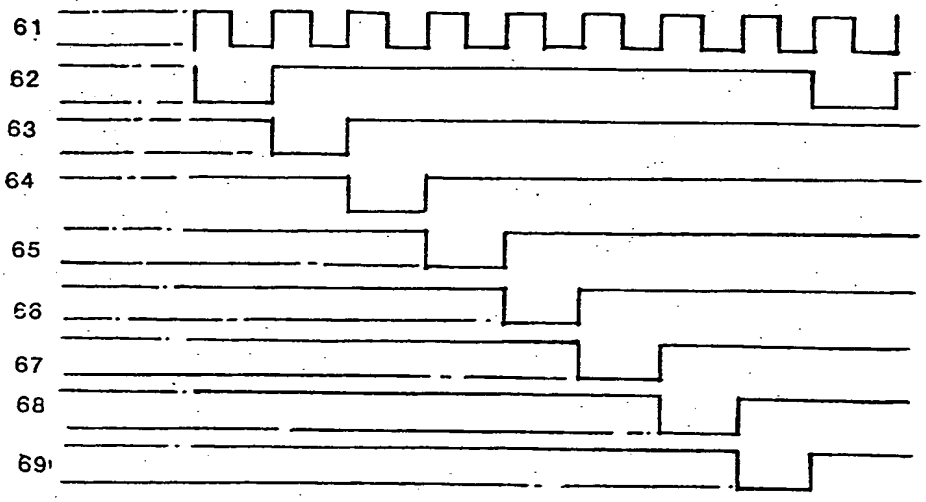


FIG.6

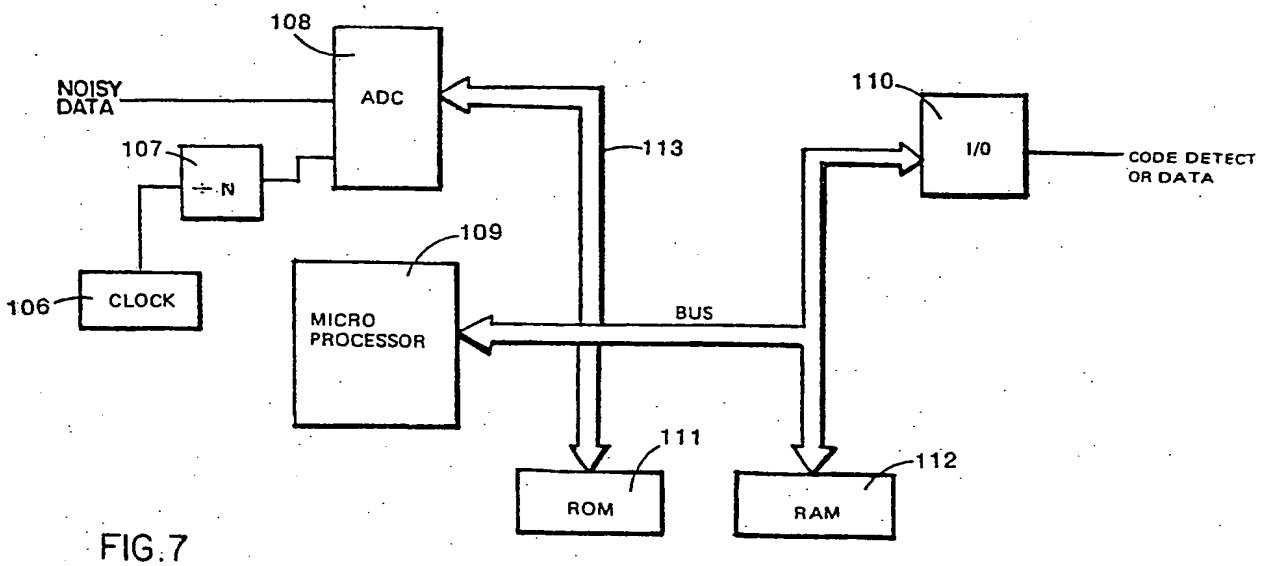


FIG.7

MICROPROCESSOR IMPLEMENTATION

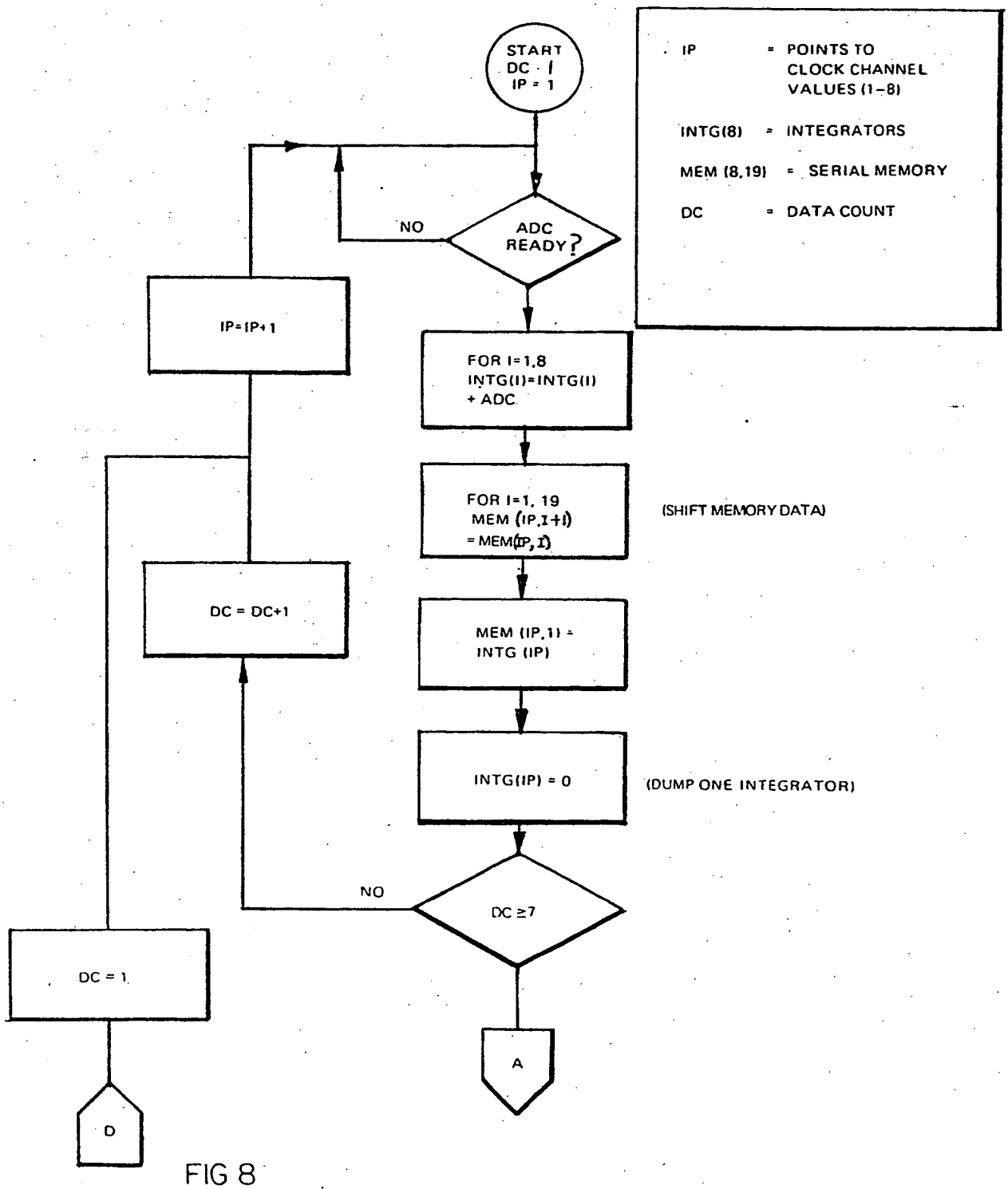
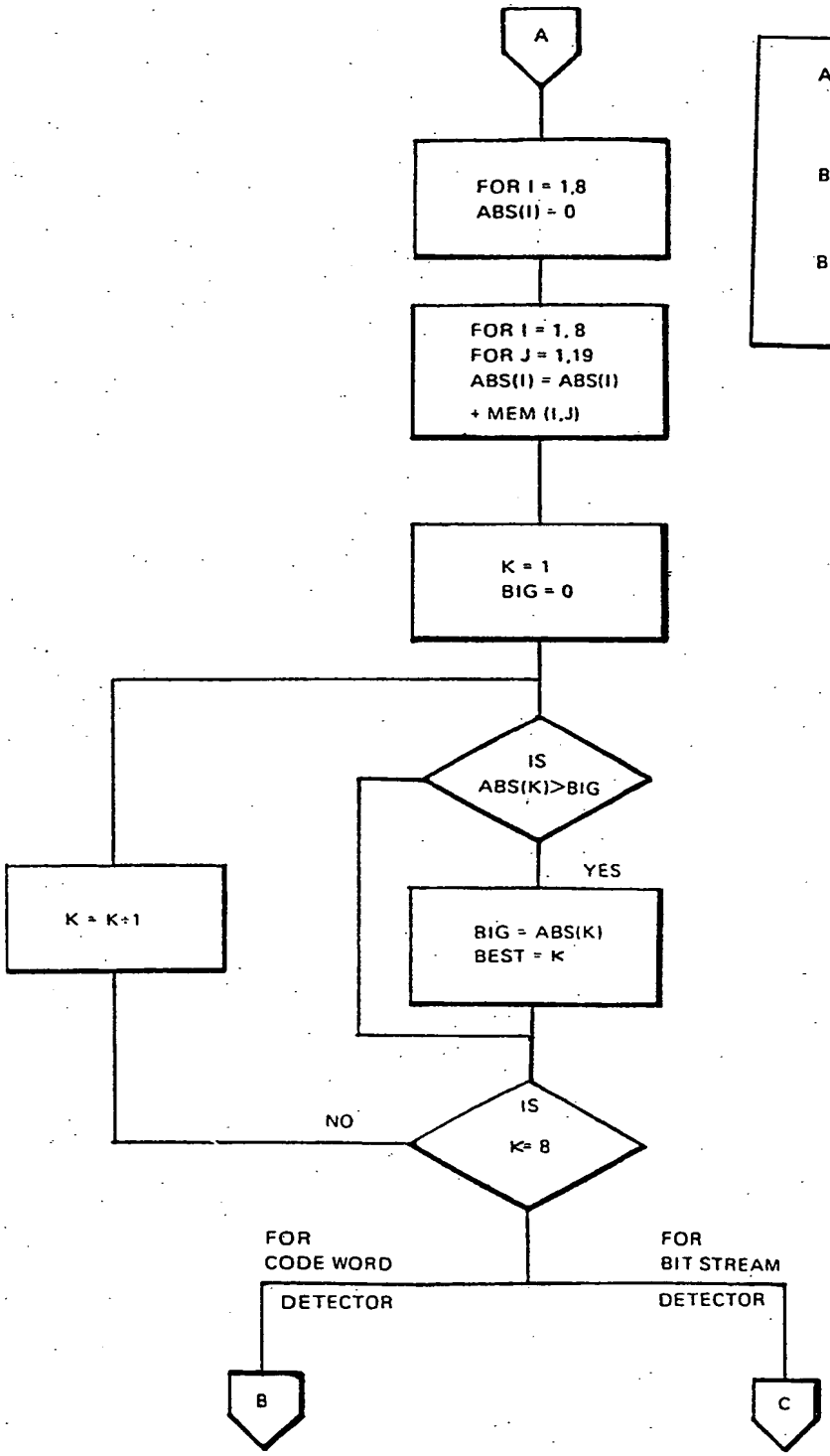

START
DC = 1
IP = 1
NO
ADC READY?
IP=IP+1
FOR I=1,8
INTG(I)=INTG(I)
+ ADC
FOR I=1, 19
MEM (IP,I+1)
= MEM(IP,I)
(SHIFT MEMORY DATA)
DC = DC+1
MEM (IP,1) =
INTG (IP)
INTG(IP) = 0
(DUMP ONE INTEGRATOR)
NO
DC ≥7
DC = 1
A
D
IP = POINTS TO CLOCK CHANNEL VALUES (1-8)
INTG(8) = INTEGRATORS
MEM (8,19) = SERIAL MEMORY
DC = DATA COUNT

FIG 8



ABS(8) SUM ABSOLUTE VALUE OF DATA IN SERIAL MEMORY

BIG = VALUE OF BIGGEST ABS(X)

BEST = POINTS TO BIGGEST SUMMED ABSOLUTE VALUE

FIG. 9

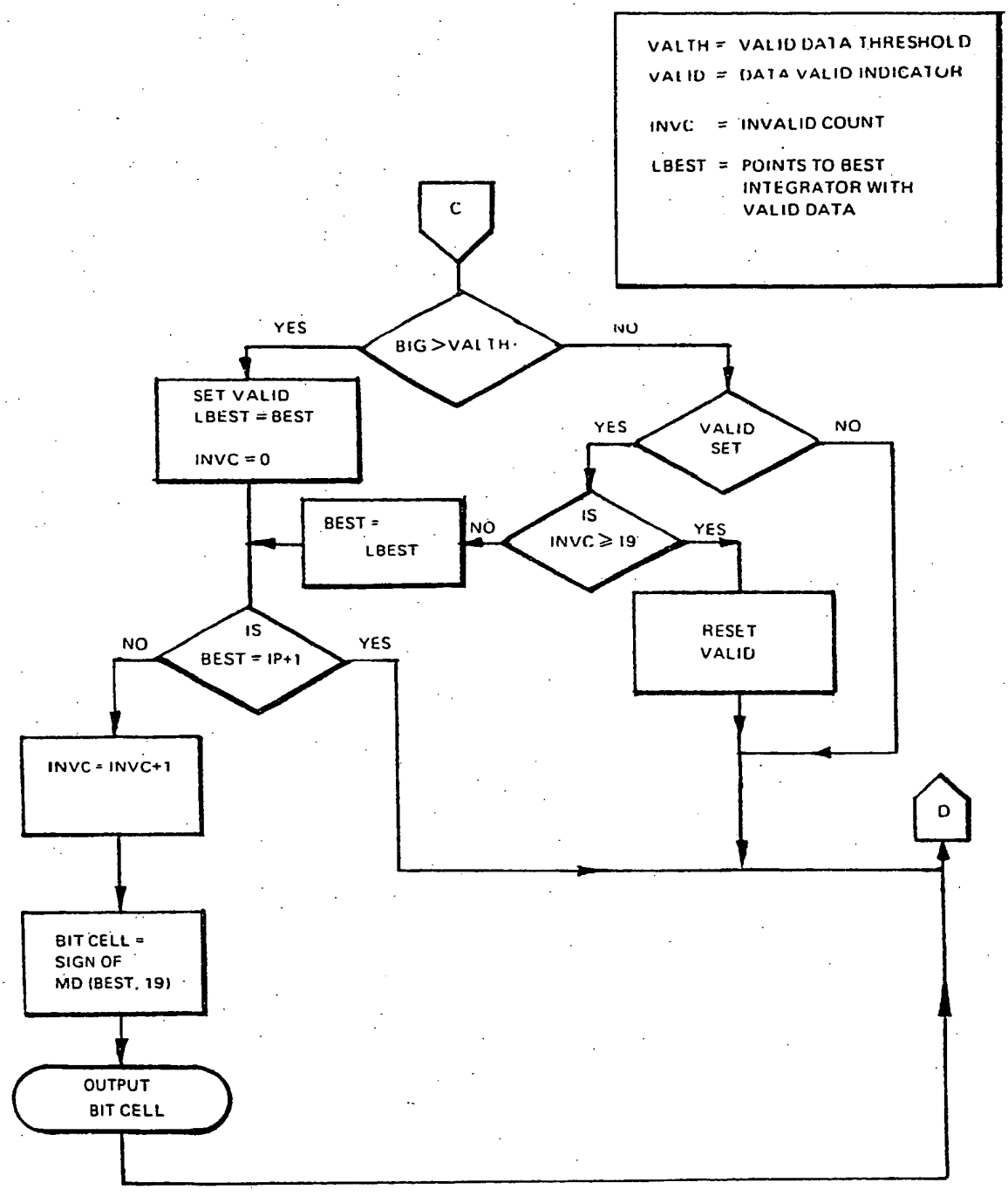

VALTH = VALID DATA THRESHOLD
VALID = DATA VALID INDICATOR
INVC = INVALID COUNT
LBEST = POINTS TO BEST INTEGRATOR WITH VALID DATA
C
BIG > VALTH
YES
NO
SET VALID
LBEST = BEST
INVC = 0
VALID SET
YES
NO
IS INVC ≥ 19
YES
NO
BEST = LBEST
RESET VALID
IS BEST = IP+1
NO
YES
INVC = INVC+1
D
BIT CELL = SIGN OF MD (BEST, 19)
OUTPUT BIT CELL

FIG. 10

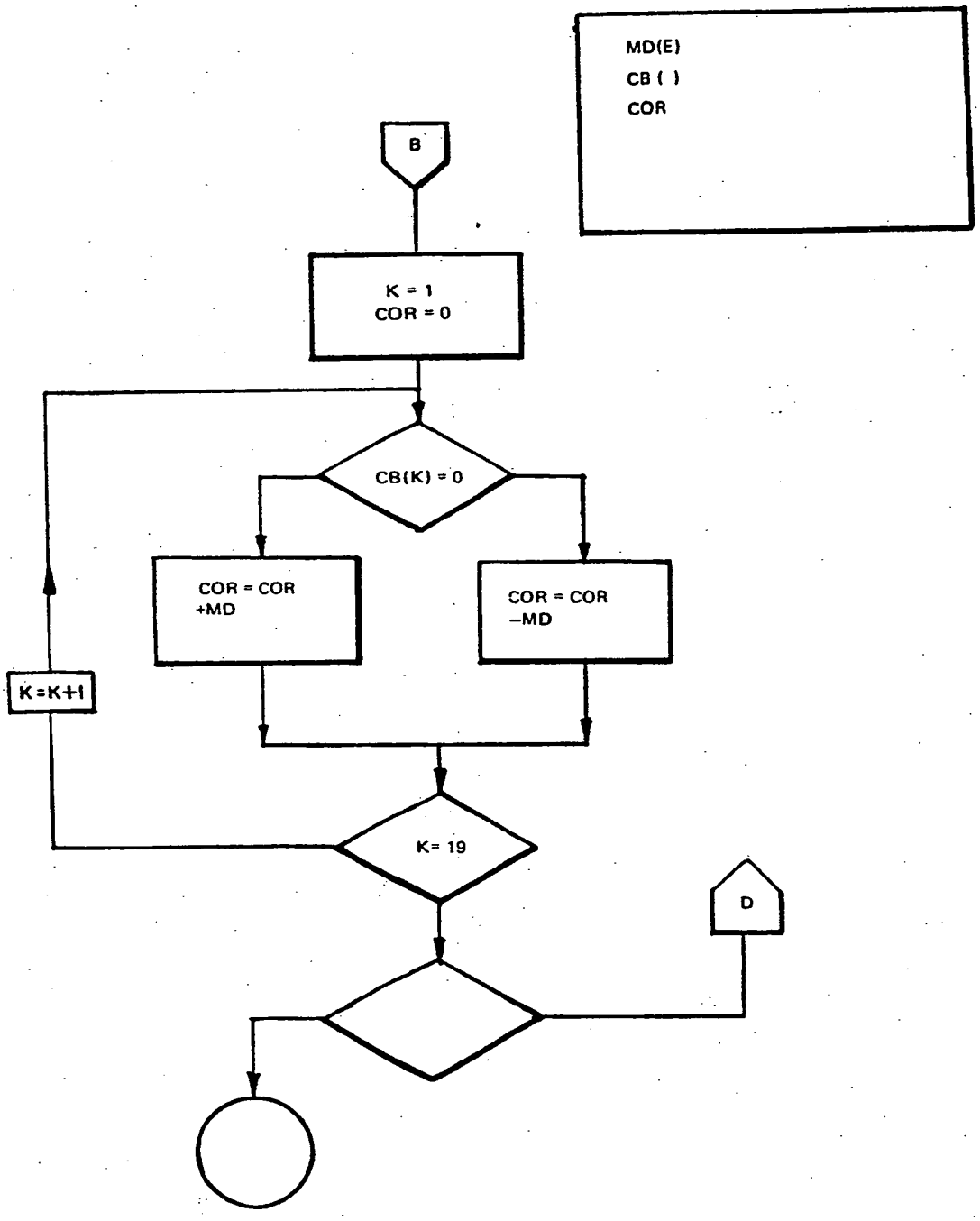


FIG.11

European Patent Office

EUROPEAN SEARCH REPORT

Application number
EP 81 10 4498

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim
X	IEEE TRANSACTIONS ON AEROSPACE AND ELECTRONIC SYSTEMS, vol AES-5, no. 3, May 1969, New York, US A.L. McBRIDE et al. "Optimum estimation of bit synchronization" pages 525-536. * Page 531, left-hand column, line 13 - right-hand column, line 6; figures 4,5 *	1-5
	--	
	US - A - 3 701 894 (E.M. LOW) * Column 4, line 61 - column 5, line 59; figure 2 *	1,3-5, 8

CLASSIFICATION OF THE APPLICATION (Int. Cl.³)

H 04 L 7/02

TECHNICAL FIELDS SEARCHED (Int. Cl.³)

H 04 L 7/02

CATEGORY OF CITED DOCUMENTS

X: particularly relevant
A: technological background
O: non-written disclosure
P: intermediate document
T: theory or principle underlying the invention
E: conflicting application
D: document cited in the application
L: citation for other reasons

&: member of the same patent family, corresponding document

X The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	09-10-1981	STRASSEN

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